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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,095	03/30/2001	Koichi Hashimoto	740250-837	2229

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EXAMINER	
DIVINE, LUCAS	

ART UNIT	PAPER NUMBER
2624	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/821,095	HASHIMOTO ET AL.	
	Examiner	Art Unit	
	Lucas Divine	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/13/05 has been entered.

Response to Amendment

2. Claims 1 – 5 are pending.

Response to Arguments

3. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ibaraki (US 5617476) in view of well known prior art.

Regarding claim 1, Ibaraki teaches **an image processing apparatus comprising at least two signal processor modules interconnected each other in series** (Fig. 8A, 81 and 82 connected in series by processed data connection)**, each of the signal processor modules having an input port through which data is input** (sample data input to 81, processed data input to 82)**, and an output port through which data is output** (81 outputs processed data, 82 further processed data to 83)**, wherein at least one of the signal processor modules outputs both unprocessed input data and processed data obtained by processing the input data** (81 outputs both unprocessed and processed data on two parallel lines, col. 12 lines 27-41)**.**

Ibaraki teaches the functional blocks 81 and 82 for performing specific computer functions but does not specifically discuss the physical implementations.

However, well-known prior art teaches that a functional block that performs computer functions can have a memory for storing a program and a processor for executing the program.

It would have been obvious to one of ordinary skill in the art that the functional blocks 81 and 82 to be implemented including memories including programs and processors to run the programs. The motivation for doing so would have been to have specific code and processor units that are optimized for each specific task of each functional block.

6. Claims 2 – 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ibakari in view of Ahamed et al. (US 5978831).

Regarding claim 2, which depends from claim 1, Ibakari further teaches

said at least one of the signal processor modules 81:

stores unprocessed input data as input through the input port (81 implicitly stores the unprocessed data in some sort of buffer/memory in order to perform the output of unprocessed data; col. 12 line 35) **and processed data obtained by reading out and processing unprocessed input data stored in the memory** (81 implicitly stores the processed data output in some sort of buffer/memory in order to perform the output of processed data; col. 12 line 33) **and**

outputs through the output port unprocessed data and processed data stored in the memory (col. 12 lines 30-40 teach the outputting of unprocessed data and processed data stored in separator 81), **and**

the other signal processor module(s) 82:

stores in the memory unprocessed input data as input through the input port (82 implicitly stores unprocessed data [i.e. hasn't been block encrypted yet] in order to perform processing on it as discussed in the rejection of claim 1) **and processed data obtained by reading out and processing unprocessed input data stored in the memory** (82 implicitly stores processed data and processes the data by reading from the implicit memory, processing, and writing back to memory as standard processing technique known to those of ordinary skill in the art; processing discussed in col. 12 line 36) **and**

outputs through the output port processed data stored in the memory (Fig. 8A, 82 outputs encrypted 'processed' data to 83).

While Ibaraki teaches processor modules receiving, processing, and outputting data, Ibaraki does not specifically teach the **input, processing, and output as being controlled synchronously within cycles.**

Ahamed teaches the **input, processing, and output as being controlled synchronously within cycles** (Fig. 7 clock 21 which controls the data transfers of the processors by the unit of clock cycles).

It would have been obvious to add the synchronous behavior of Ahamed to the system of Ibaraki. The motivation for doing so would have been to coordinate data transfers between modules of differing processing speeds better than asynchronously (col. 3 lines 3-8). Other advantages of synchronous – clock driven – processor modules are well known in the art.

Regarding claim 3, which depends from claim 2, Ahamed further teaches **a synchronous circuit which causes data transfer for signal processor modules to occur in synchronization with clocks which are the same in phase and frequency** (Fig. 7 clk 21 causes data transfers for processor modules 11 and 12).

Regarding claim 4, which depends from claim 3, Ibaraki further teaches **the data transfer widths between the signal processor modules are equal to each other** (there is only one data transfer width between the signal processors [processed data signal between 81 and 82]) **and**

Ahamed further teaches **the synchronous circuit determines the frequency of the transfer clock on the basis of the data transfer rate between the pair of signal processor**

modules between which the largest amount of data is to be transferred (Ahmed teaches the determination of clk frequency based on the data transfer rate of the slow processor 11; by adding the synchronization features of Ahamed to the module transfers of Lyons as discussed in the rejection of claim 2, the determination of the clock frequency would be based on the speeds of the processor modules 132 and 136 and the amount of data between them, which would have been obvious to one of ordinary skill in the art).

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lyons as applied to claim 1 above, and further in view of Durkos et al. (US 4777590).

Regarding claim 5, which depends from claim 1, While Lyons teaches a system with multiple functional modules for performing computing tasks, Lyons does not specifically teach **a mounting means on which a signal processor module is removably mounted is provided for at least one of the signal processor modules and a switching means is provided for said at least one signal processor module to transfer data to the signal processor module through its input port when it is mounted on the mounting means and to transfer the same to a component rearward of the signal processor module when it is not mounted on the mounting means.**

Durkos teaches a system with multiple functional modules for performing computing tasks including:

a mounting means on which a signal processor module is removably mounted is provided for at least one of the signal processor modules (Fig. 4, wherein the modules 102 can be removably plugged-in 'mounted' in the system) **and**

a switching means is provided for said at least one signal processor module to transfer data to the signal processor module through its input port when it is mounted on the mounting means and to transfer the same to a component forward of the signal processor module when it is not mounted on the mounting means (Fig. 4, wherein module select circuit 56 acts as a switching means by switching which plugged-in 'mounted' modules 102 are connected to each other in the system, and when a module is not plugged-in to the system, data is routed to the next module).

It would have been obvious to one of ordinary skill in the art to provide a system with the modules of Ibaraki that are mountable as in Durkos. Durkos teaches that the modules are in series (wherein the block arrows between modules signify connections in Fig. 4) and teaches modules with different functionalities. The motivations for doing so would have been to provide for an easily customizable and upgradeable system (Durkos col. 1 lines 51-52).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lucas Divine whose telephone number is 571-272-7432. The examiner can normally be reached on Monday - Friday, 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Moore can be reached on 571-272-7437. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lucas Divine
Examiner
Art Unit 2624

ljd

KING Y. POON
PRIMARY EXAMINER